EL323//El324 Digital System Laboratory II

LAB 1 : Introduction to DE-0 With Quartus II

Objective:

1. To know the ALTERA DE-0.
2. Can use the Quartus II and create the new project using VHDL and Schematic/Block diagram.
3. To know the assign pin of DE-0 in Quartus.
4. To know the compiling of DE-0.
5. Can programmable the DE-0 with VHDL file.

Part I: Start a new Project

1. Open the Quartus II that in the desktop. The program should be in fig 1.

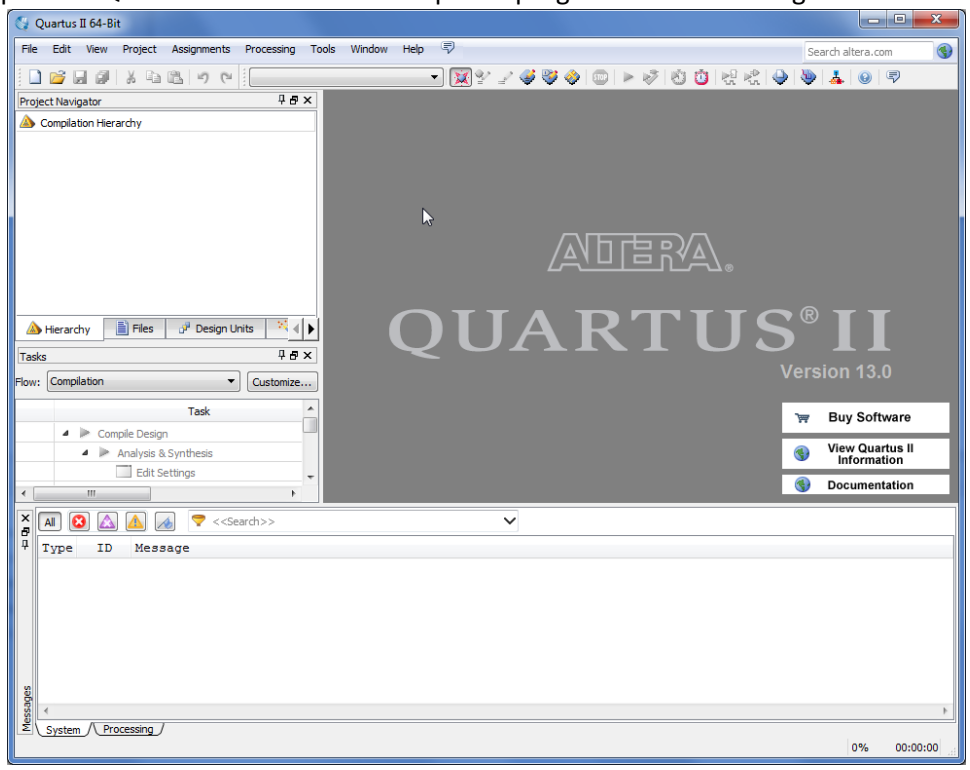


Fig 1. The main Quartus II display.

2. Select File > New Project Wizard and click Next. The program should be in fig 2. Then you can chose the directory to save the project and select the name of the project in this step and click Next to continue.

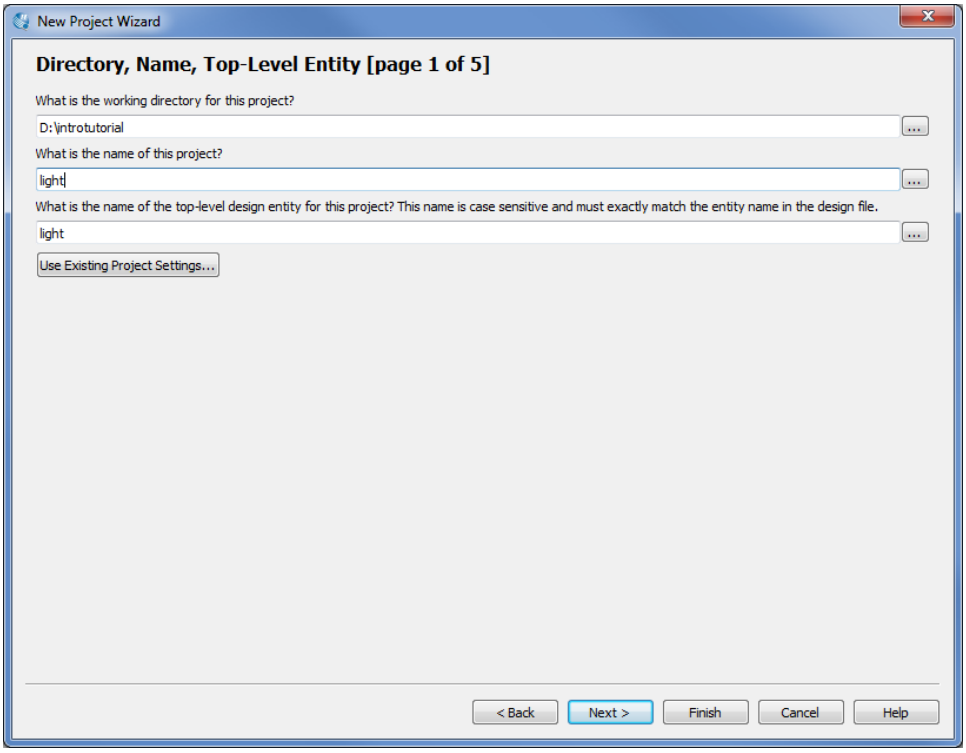


Fig 2. Creation of a new project.

3. You can add your file which exist files (if any). But in this step Click Next.

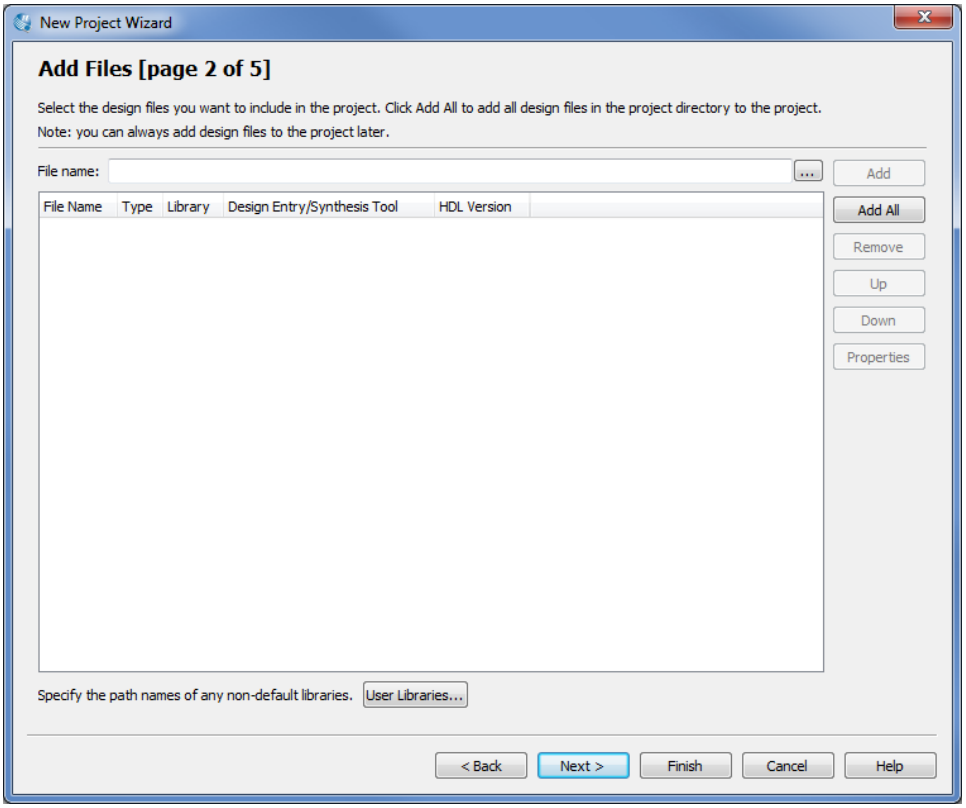


Fig 3. The wizard can include user-specified design files.

4. You should to specify the type of device which in use such as DE-0 choose the Cyclone III series EP3C16F484C6 and click Next to continue.

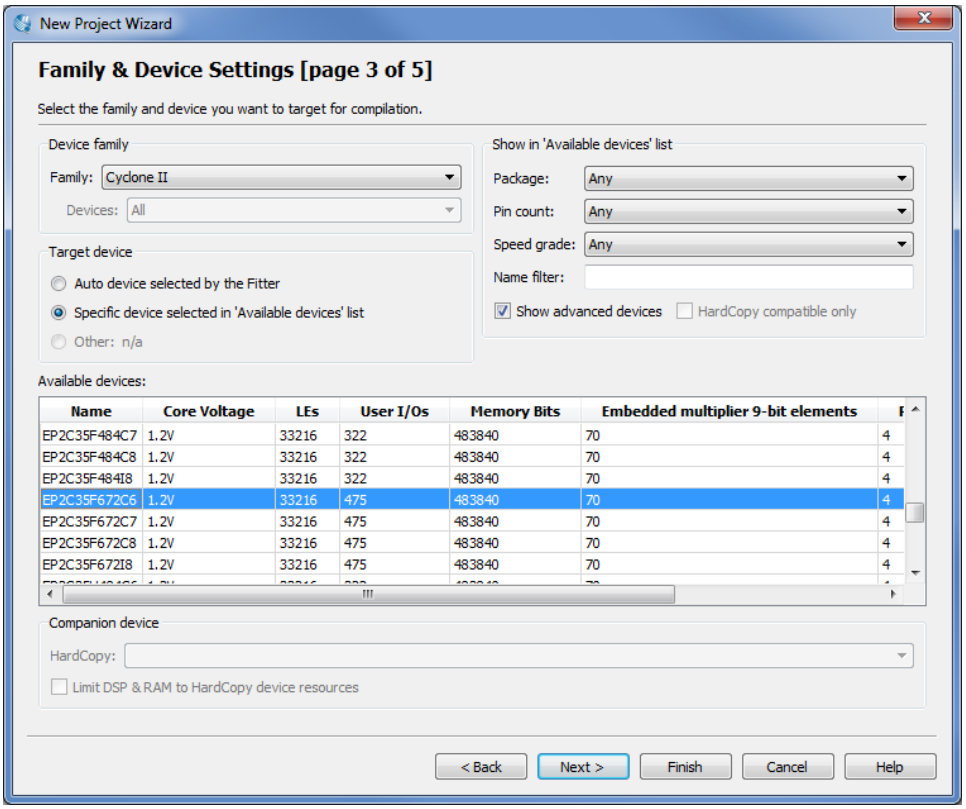


Fig 4. Choose the device family and a specific device.

5. EDA tools can specify any third-party tools that should be used. So click Next to continue.

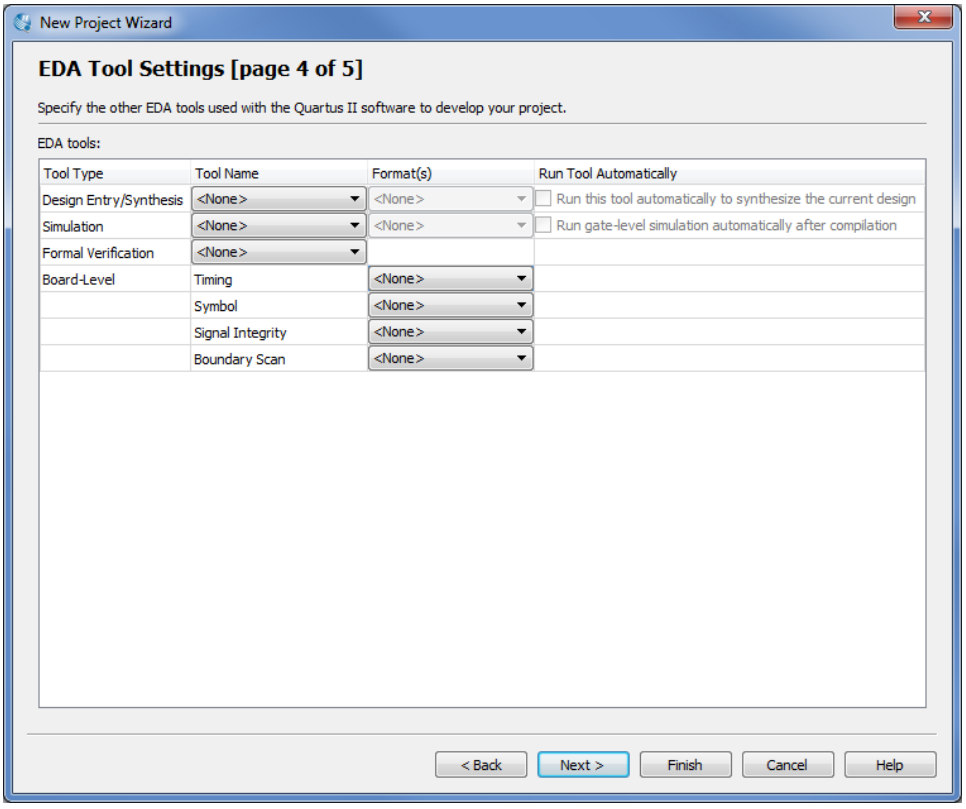


Fig 5. Other EDA tools can be specified.

6. The Summary of the project setting Click Finish to continue.

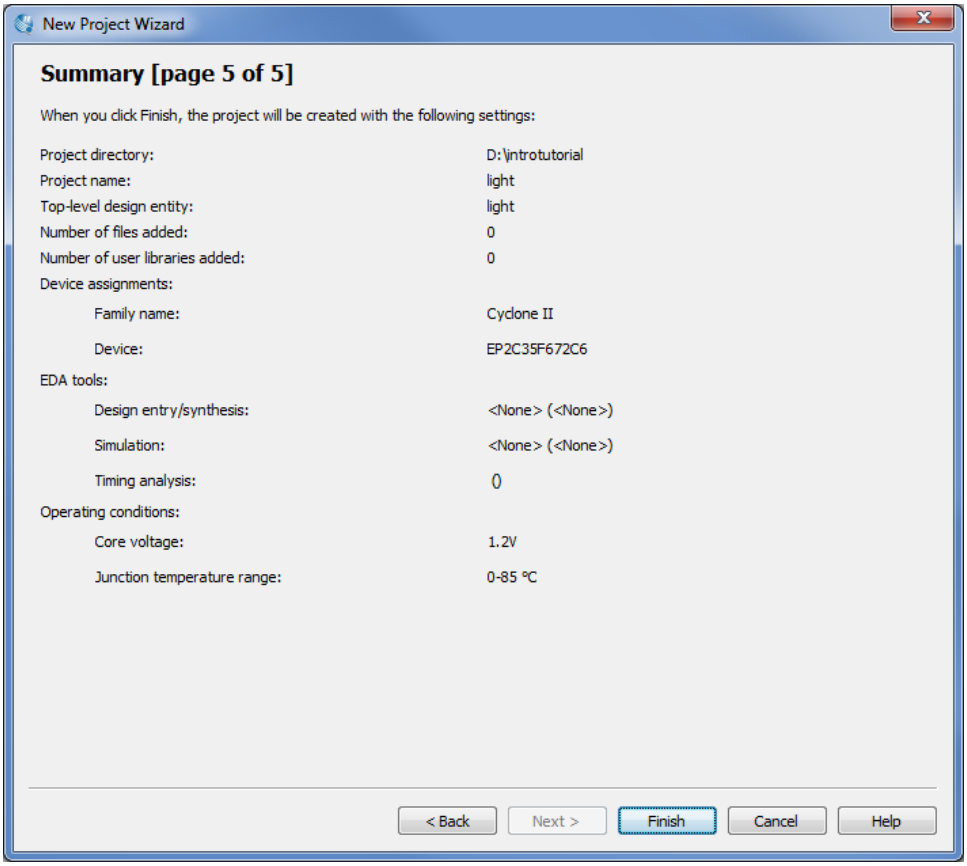


Fig 6. Summary of project settings.

7. The display of program after created project.

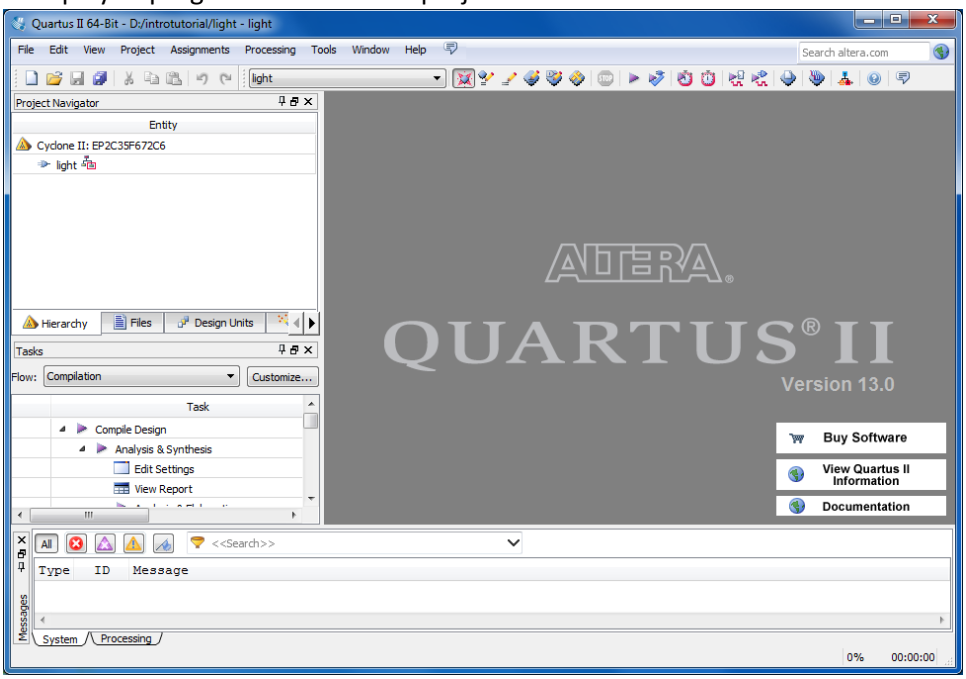


Fig 7. The Quartus II after created project.

8. After created project, you should desired to use VHDL or Schematic/Block diagram. Select File>New In Design Files select you want to use VHDL Files or Block diagram/Schematic.

Part II: Assignment Default Pin

1. The assignment pin should be first before to do anything. You can assign by yourself. Pin assignment are made by using Assignment Editor. To Select Assignment > Assignment Editor

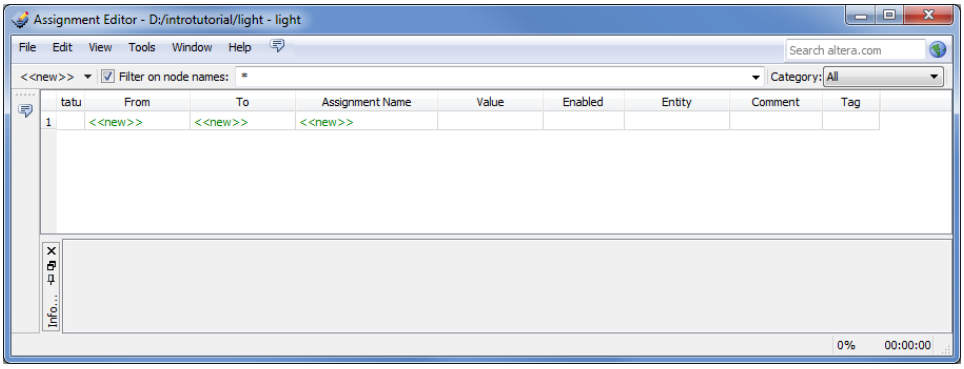


Fig 8. Assign by user.

2. Or assign by default using DE-0_assignpin_default.qsf. Select Assignment > Import Assignments and to find the DE-0_assignpin_default.qsf Then Click Ok.

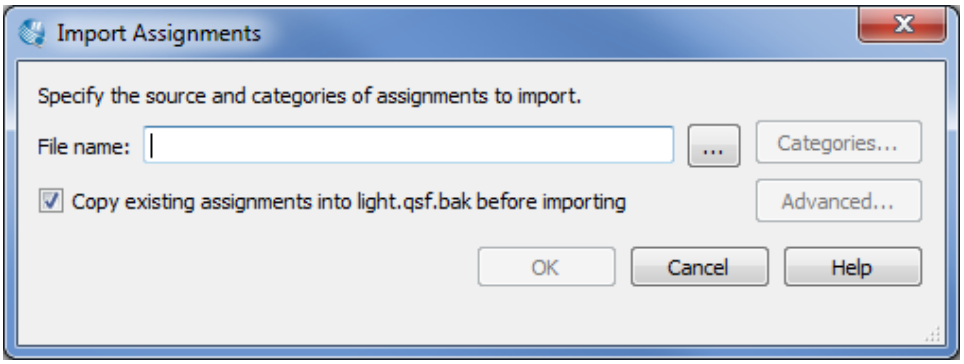


Fig 9. Assign by default.

Part III: Schematic Design

1. Right at the space select Insert>Symbol

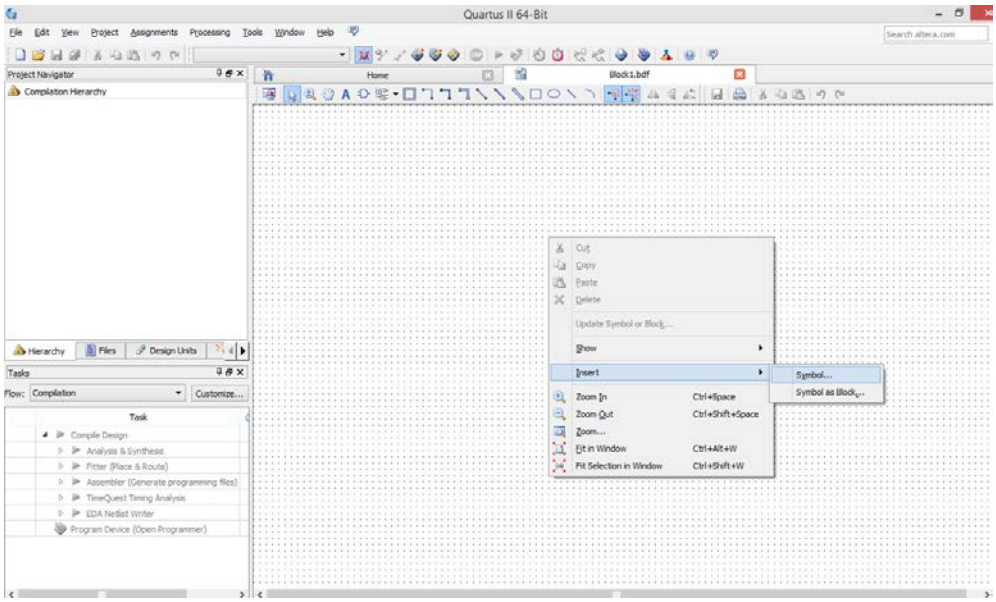


Fig 10. Insert symbol

2. Search the name of item by type such as “and2” then click Ok to continue.

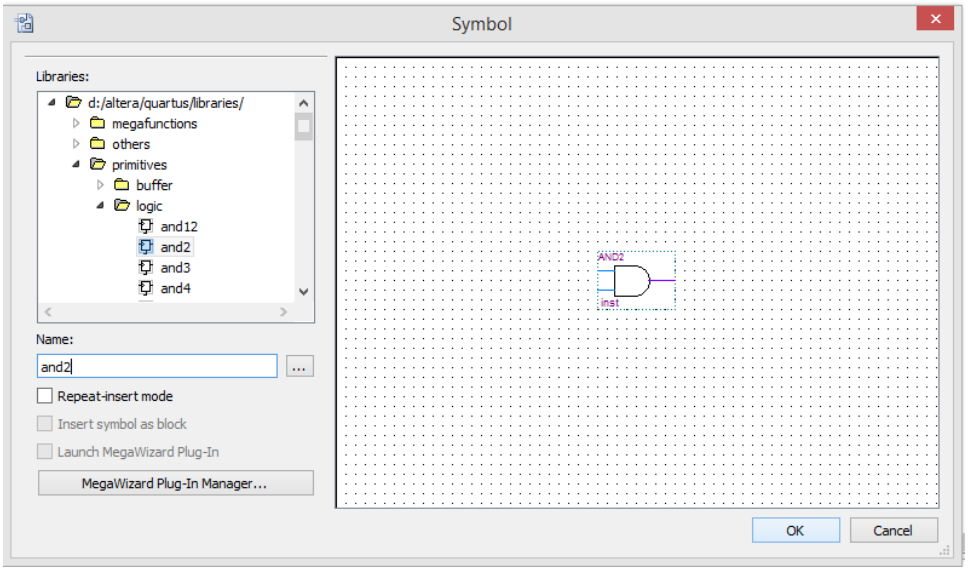


Fig 11. Browse Symbol

3. Placed the selected item in a space.

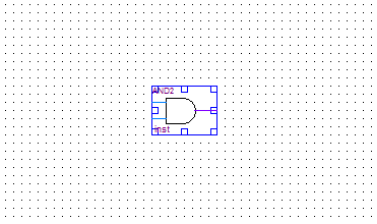


Fig 12. Symbol

4. Completed the circuit by insert the input and output with wired.

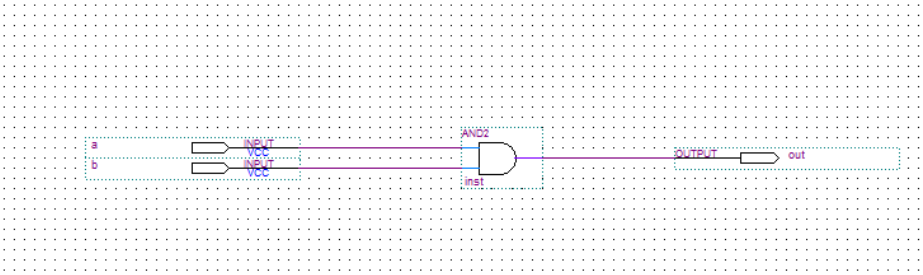


Fig 13. Completed Circuit.

Part IV: Compiling DE-0

1. Run the Compiler by selecting Processing > Start Compilation. The Result should not any error.

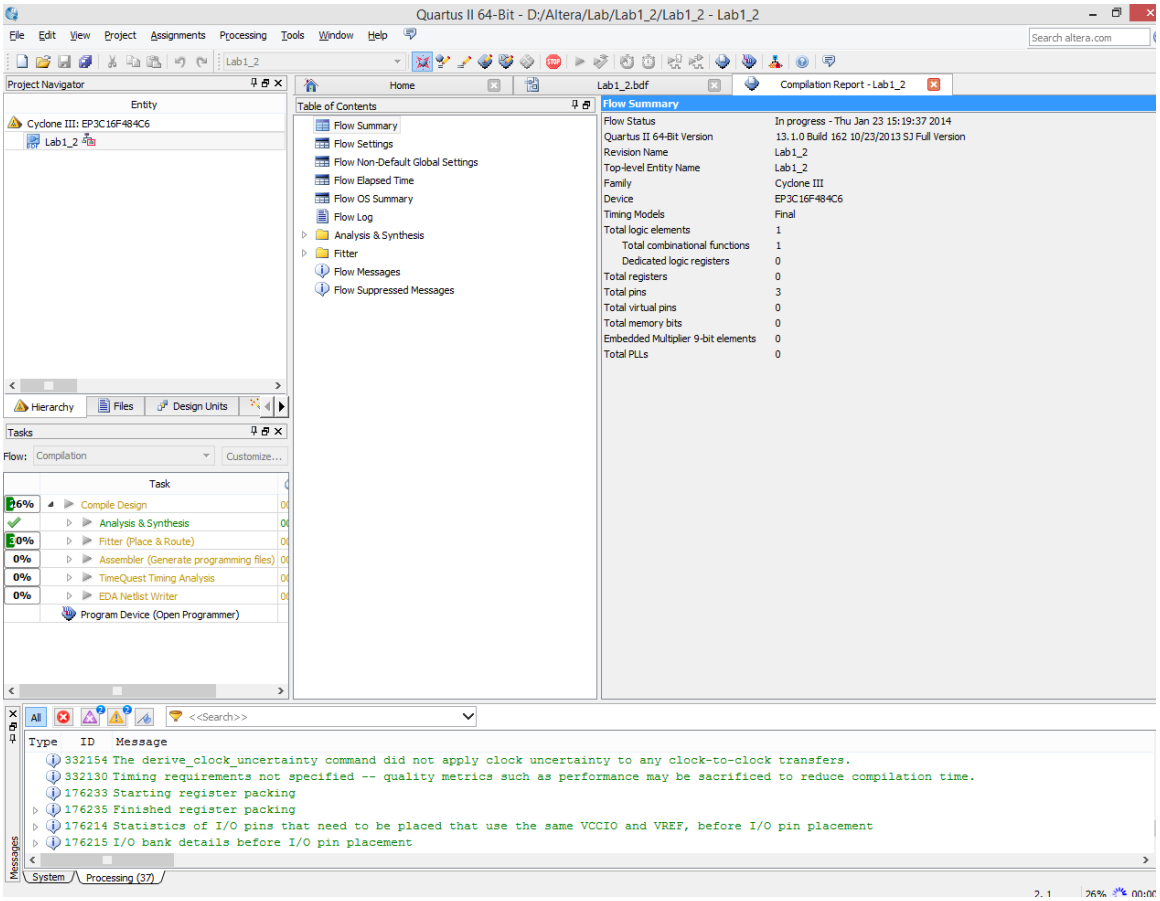


Fig 14. The Compiling Screen.

Part V: Programming DE-0

1. Flip the RUN/PROG switch into the RUN position. Select Tools >Programmer that should like fig 10.

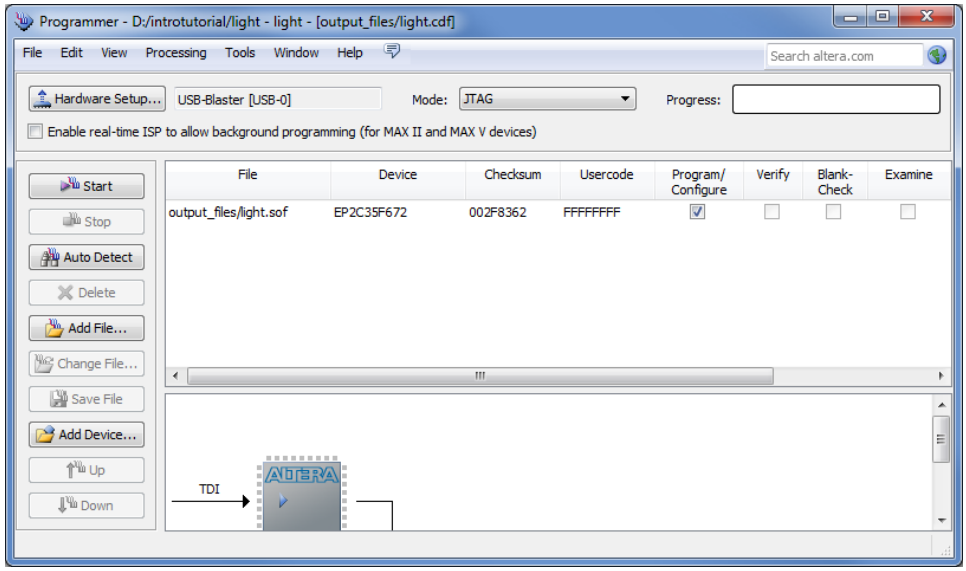


Fig 15. The Programmer window.

2. If Hardware setup not chose the USB-Blaster Click Hardware Setup and Chose it that like Fig 11.

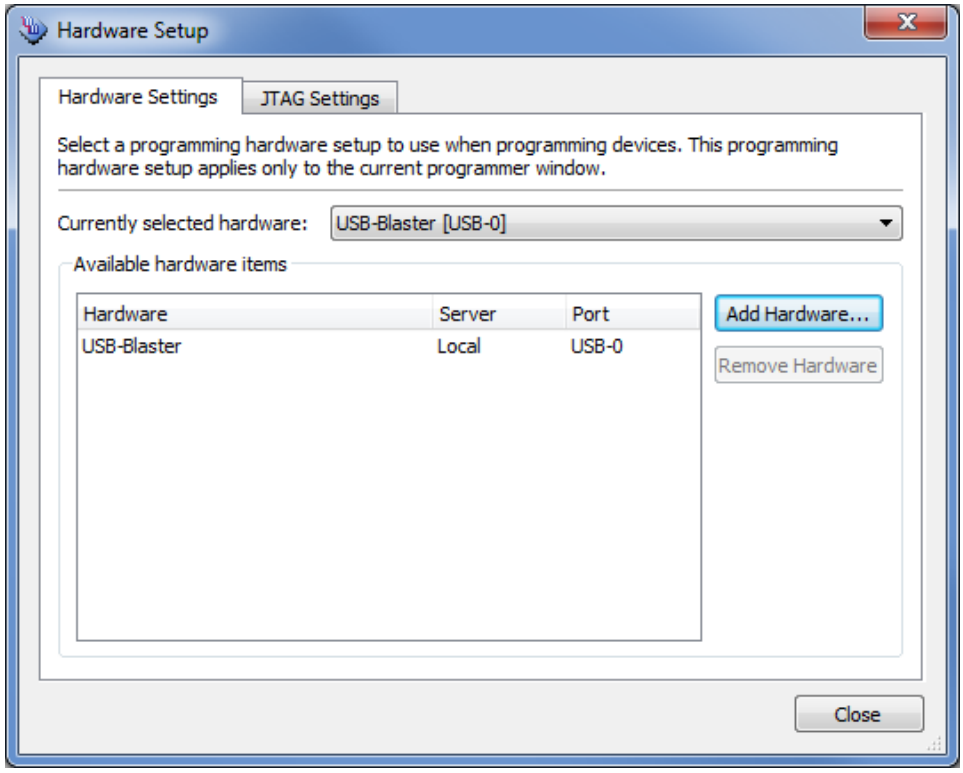


Fig 16. The Hardware Setup window.

3. The Programmer listed file in the window in fig 10. If the file not already listed the click Add file and select it. The file should in the output_files and look like the project name which in *.sof file. And checked Program/Configure then Start to program to DE-0.

Exercise I: Use Schematic/Block Diagram

1. Create new project name : Lab1_1 and then select the schematic/block diagram.
2. Draft the schematic look like Fig 12.

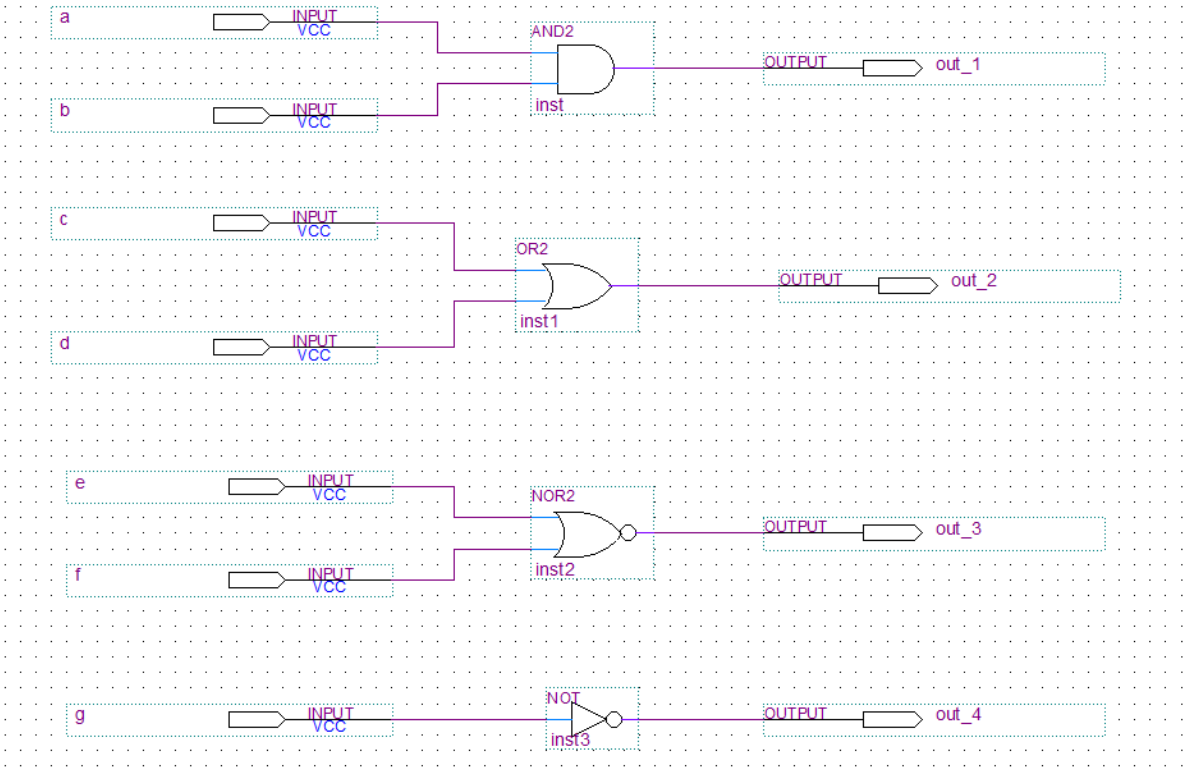


Fig 12. Exercise Schematic

3. Compile this project
4. Simulation waveform editor like Fig 13.

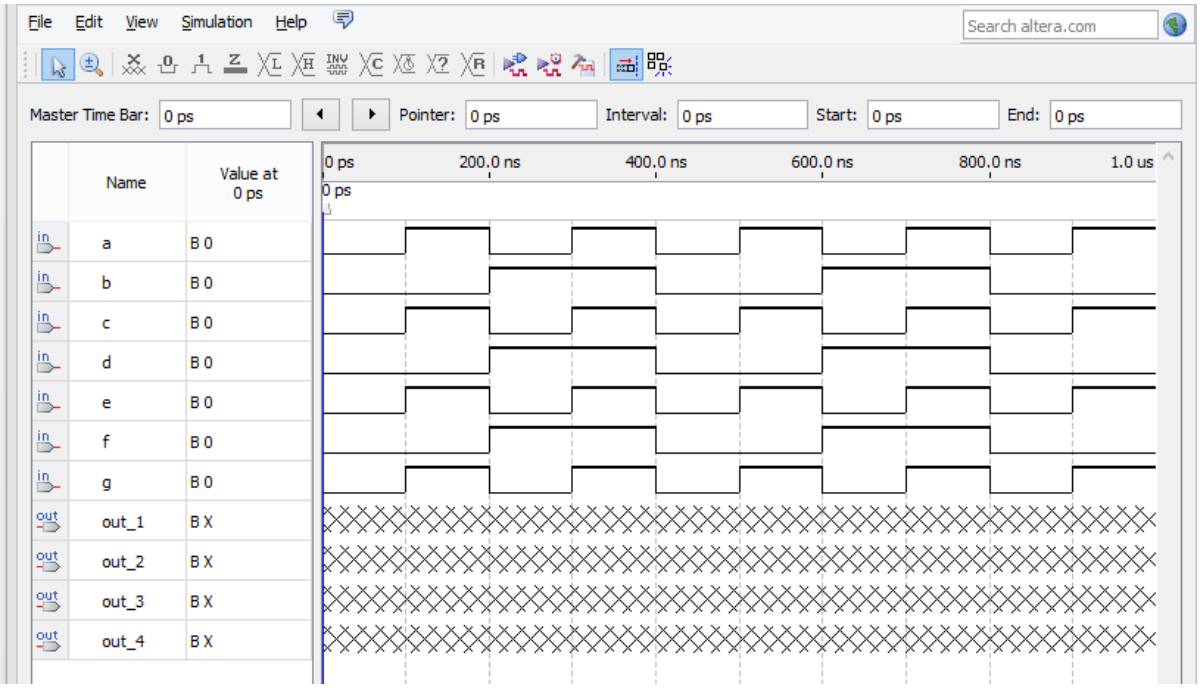


Fig 13.

5. Full Fill in this table

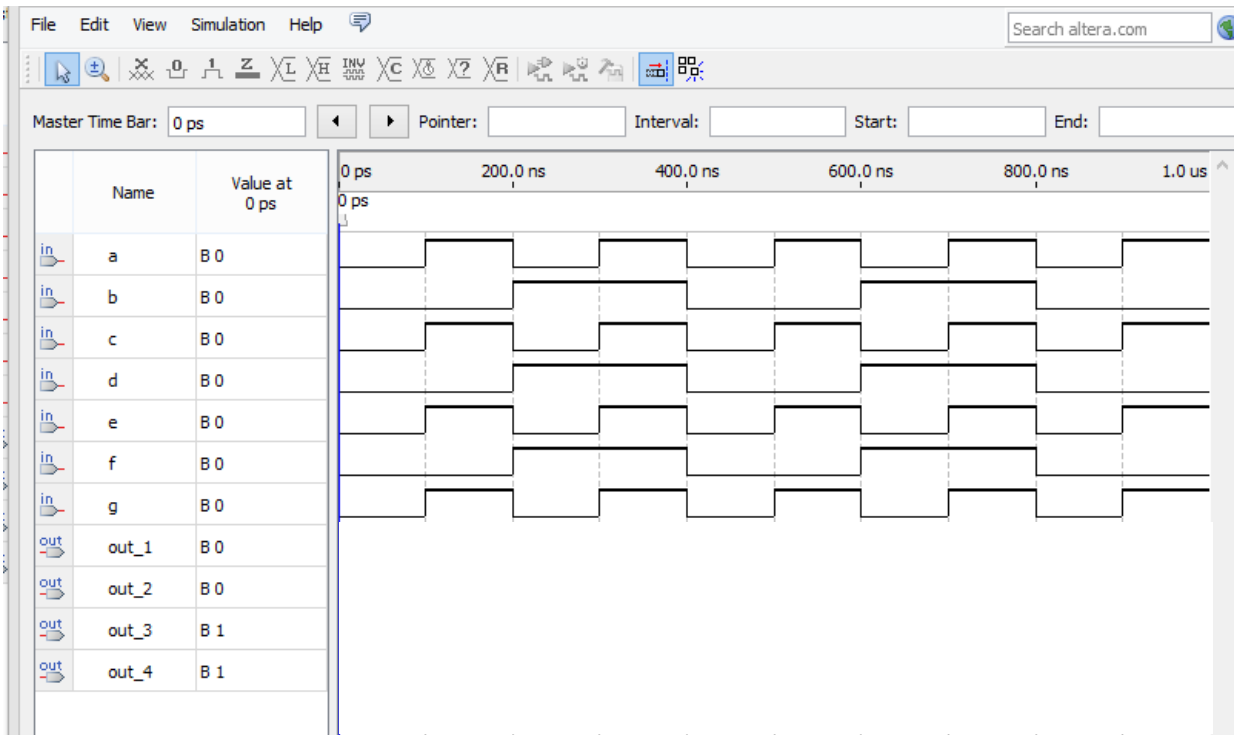
	A	B	Out_1
And Gate	0	0	
	0	1	
	1	0	
	1	1	

	C	D	Out_2
Or Gate	0	0	
	0	1	
	1	0	
	1	1	

	E	F	Out_3
Nor Gate	0	0	
	0	1	
	1	0	
	1	1	

	G	Out_4
Not Gate	0	
	1	

Result



Conclusion

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Exercise II: Use VHDL

1. Create new project name : Lab1_2 and then select VHDL Files.
2. Code the project as

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
-- Simple module that connects the SW switches to the LEDG lights
ENTITY Lab1_2 IS
PORT ( SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);
LEDG : OUT STD_LOGIC_VECTOR(9 DOWNTO 0)); -- green LEDs
END Lab1_2;
ARCHITECTURE Behavior OF Lab1_2 IS
BEGIN
LEDG <= SW;
END Behavior
```

3. Assign Pin of DE-0 in *Part II: Assignment Pin DE-0*
4. Compile this project

Result

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Conclusion

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