EL323//El324 Digital System Laboratory II

LAB 4 : Behavioral and Dataflow VHDL

Objective:

1. Can use the Quartus II and create the new project using VHDL
2. To know the assign pin of DE-0 in Quartus.
3. Design using VHDL
4. To know the different between the behavioral and dataflow structure.

• Behavioral – describes how the output is derived from the inputs using structured statements.

• Dataflow – describes how the data flows from the inputs to the output most often using NOT, AND and OR operations.

LAB 4.1 Hex7seg as VHDL Dataflow

1. Create new Project name Lab4_1.
2. Create new entity for 7-segment display in this below

SW3	SW2	SW1	SW0	Hex7seg
0	0	0	0	F
0	0	0	1	E
0	0	1	0	d
0	0	1	1	C
0	1	0	0	b
0	1	0	1	A
0	1	1	0	9
0	1	1	1	8
1	0	0	0	7
1	0	0	1	6
1	0	1	0	5
1	0	1	1	4
1	1	0	0	3
1	1	0	1	2
1	1	1	0	1
1	1	1	1	0

3. Use the DE0 User Manual to define the DE0 pin.
4. Compile the code and program to DE0.

LAB 4.1 CODE

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

-- Simple module that connects the SW switches to the LEDG lights
ENTITY Lab4_1 IS
	PORT ( SW : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
	     HEX0_D : OUT STD_LOGIC_VECTOR(6 DOWNTO 0) );
END Lab4_1;

ARCHITECTURE Behavior OF Lab4_1 IS
	SIGNAL s : STD_LOGIC_VECTOR (1 DOWNTO 0);
BEGIN
	s <= SW(1 DOWNTO 0);

	--
	--        0
	--       ---
	--      |   |
	--    5|   |1
	--      | 6 |
	--       ---
	--      |   |
	--    4|   |2
	--      |   |
	--       ---
	--        3
	--

HEX0_D(0) <= _____________________________________________
HEX0_D(1) <= _____________________________________________
HEX0_D(2) <= _____________________________________________
HEX0_D(3) <= _____________________________________________
HEX0_D(4) <= _____________________________________________
HEX0_D(5) <= _____________________________________________
HEX0_D(6) <= _____________________________________________
	---- some additional VHDL code as necessary ----
END Behavior;
```

Lab4.1 Answer Sheet

SW				Display 7 Segment	
SW3	SW2	SW1	SW0	Character	bit HEX0_D
0	0	0	0	F	_ _ _ _ _ _ _
0	0	0	1	E	_ _ _ _ _ _ _
0	0	1	0	d	_ _ _ _ _ _ _
0	0	1	1	C	_ _ _ _ _ _ _
0	1	0	0	b	_ _ _ _ _ _ _
0	1	0	1	A	_ _ _ _ _ _ _
0	1	1	0	9	_ _ _ _ _ _ _
0	1	1	1	8	_ _ _ _ _ _ _
1	0	0	0	7	_ _ _ _ _ _ _
1	0	0	1	6	_ _ _ _ _ _ _
1	0	1	0	5	_ _ _ _ _ _ _
1	0	1	1	4	_ _ _ _ _ _ _
1	1	0	0	3	_ _ _ _ _ _ _
1	1	0	1	2	_ _ _ _ _ _ _
1	1	1	0	1	_ _ _ _ _ _ _
1	1	1	1	0	_ _ _ _ _ _ _

HEX0_D(0) <=

_____

_____

HEX0_D(1) <=

_____

_____

HEX0_D(2) <=

_____

_____

HEX0_D(3) <=

_____

_____

HEX0_D(4) <=

_____

_____

HEX0_D(5) <=

_____

_____

HEX0_D(6) <=

_____

_____

Conclusion

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LAB 4.2 Hex7seg as VHDL Behavioral

1. Create new Project name Lab4_2.
2. Create new entity for 7-segment display in this below

SW3	SW2	SW1	SW0	Hex0_D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	b
1	1	0	0	C
1	1	0	1	d
1	1	1	0	E
1	1	1	1	F

3. Use the DE0 User Manual to define the DE0 pin.
4. Compile the code and program to DE0.

LAB 4.2 CODE

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

-- Simple module that connects the SW switches to the LEDG lights
ENTITY Lab4_1 IS
	PORT ( SW : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
	    HEX0_D : OUT STD_LOGIC_VECTOR(6 DOWNTO 0) );
END Lab4_1;

ARCHITECTURE Behavior OF Lab4_1 IS
BEGIN
	PROCESS (SW)
	BEGIN
	--
	--       0
	--       ---
	--      |    |
	--    5|    |1
	--      | 6  |
	--      ---
	--      |    |
	--    4|    |2
```

```
--       |     |
--         ---
--        3
--
IF (SW = "0000") THEN   HEX0_D <= "1000000";
ELSIF (SW = "0001") THEN  HEX0_D <= " 1111001";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSIF (SW = "____") THEN  HEX0_D <= "________";
ELSE  HEX0_D <= "1111111";
END IF;
END PROCESS;


---- some additional VHDL code as necessary ----
END Behavior;
```

Lab4.2 Answer Sheet

SW				Display 7 Segment	
SW3	SW2	SW1	SW0	Character	bits HEX0_D
0	0	0	0	0	_ _ _ _ _ _ _
0	0	0	1	1	_ _ _ _ _ _ _
0	0	1	0	2	_ _ _ _ _ _ _
0	0	1	1	3	_ _ _ _ _ _ _
0	1	0	0	4	_ _ _ _ _ _ _
0	1	0	1	5	_ _ _ _ _ _ _
0	1	1	0	6	_ _ _ _ _ _ _
0	1	1	1	7	_ _ _ _ _ _ _
1	0	0	0	8	_ _ _ _ _ _ _
1	0	0	1	9	_ _ _ _ _ _ _
1	0	1	0	A	_ _ _ _ _ _ _
1	0	1	1	b	_ _ _ _ _ _ _
1	1	0	0	C	_ _ _ _ _ _ _
1	1	0	1	d	_ _ _ _ _ _ _
1	1	1	0	E	_ _ _ _ _ _ _
1	1	1	1	F	_ _ _ _ _ _ _

<u>CODE</u>   IF (SW = "0000") THEN   HEX0_D <= "1000000";

```
ELSIF (SW = "0001") THEN  HEX0_D <= "1111001";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSIF (SW = "____") THEN  HEX0_D <= "_________";
ELSE  HEX0_D <= "1111111";
```

Conclusion

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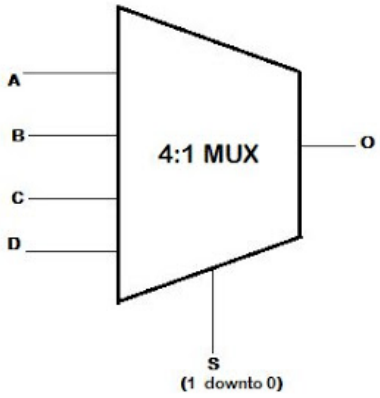
LAB 4.3 MUX 4 to 1 as VHDL Behavioral

1. Create new Project name Lab4_3.
2. Create new entity for Mux4to1 in this below

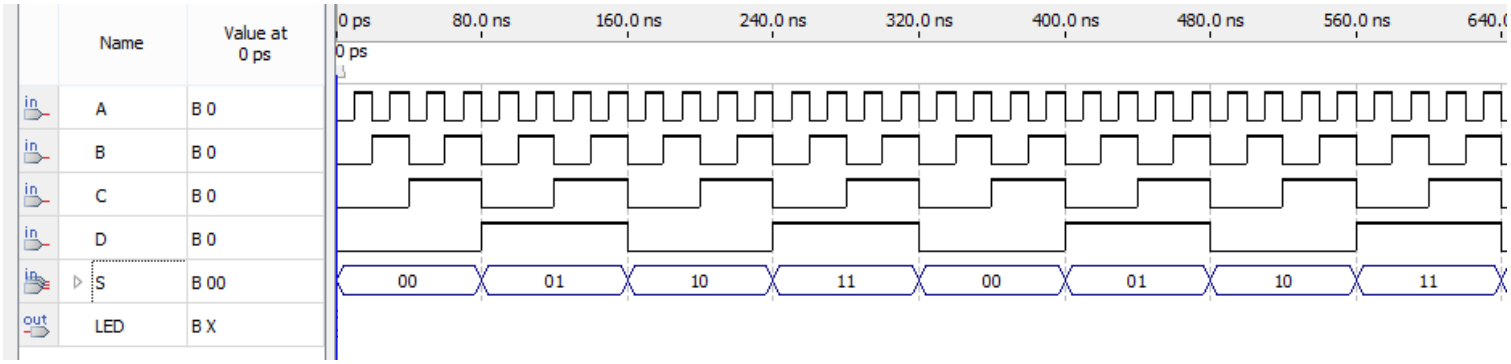


3. Use the DE0 User Manual to define the DE0 pin.
4. Compile the code and program to DE0.

LAB 4.3 CODE

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY LAB4_3 IS
PORT( A,B,C,D: IN STD_LOGIC;
    S: IN STD_LOGIC_VECTOR (1 DOWNTO 0);
    LED: OUT STD_LOGIC);
END LAB4_3;

ARCHITECTURE Behavioral OF LAB4_3  IS
BEGIN
        PROCESS(S,A,B,C,D)
        BEGIN

        CASE S IS

        WHEN "00" => LED <= A;
        WHEN "01" => LED <= B;
        WHEN "10" => LED <= C;
        WHEN OTHERS => LED <= D;

        END CASE;

END PROCESS;
END Behavioral;
```

LAB 4.3 Answer Sheet



Conclusion

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HW. Design the Multiplexer8to1 3bits as VHDL Behavioral