EL323//El324 Digital System Laboratory II

LAB 5 : Conditional Statement

Objective:

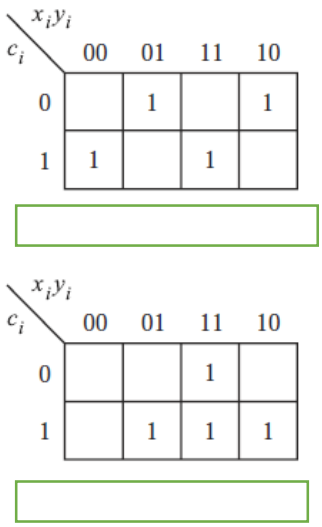
1. Can use the Quartus II and create the new project using VHDL
2. To know the assign pin of DE-0 in Quartus.
3. Design using VHDL
4. To know conditional statement and adder with 7-segment

LAB 5.1 Full Adder

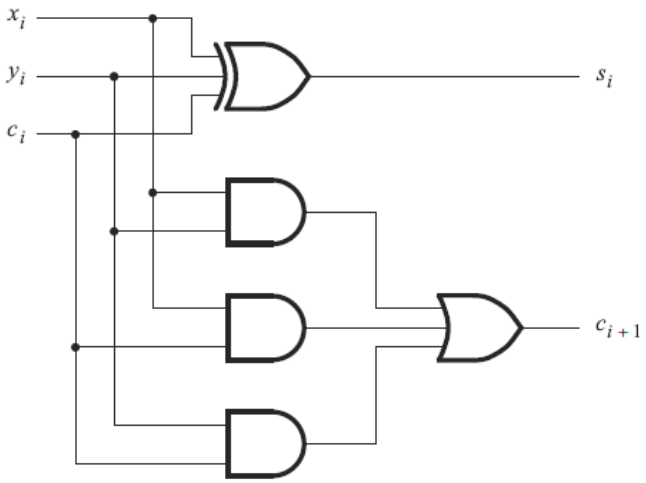
1. Create new Project name “adder”.
2. Create new entity for adder in this below

c_i	x_i	y_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) Truth table

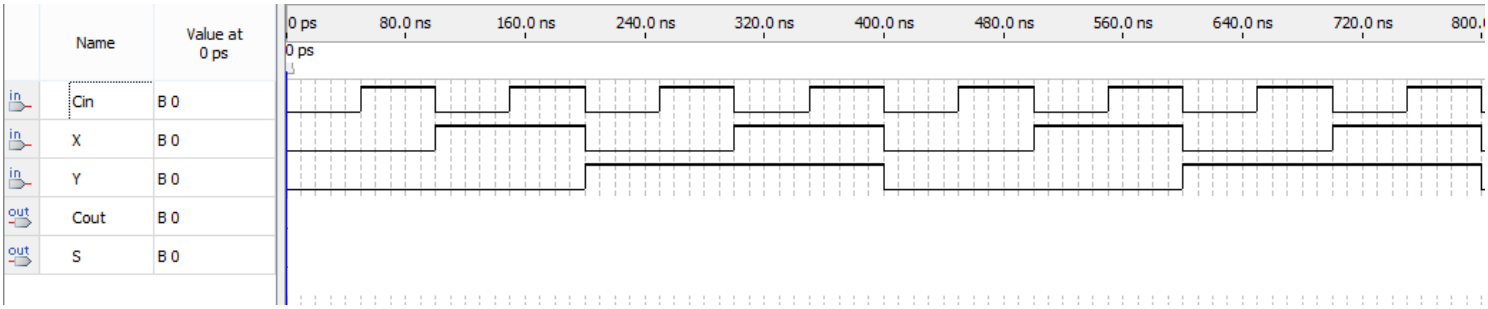


(b) Karnaugh maps



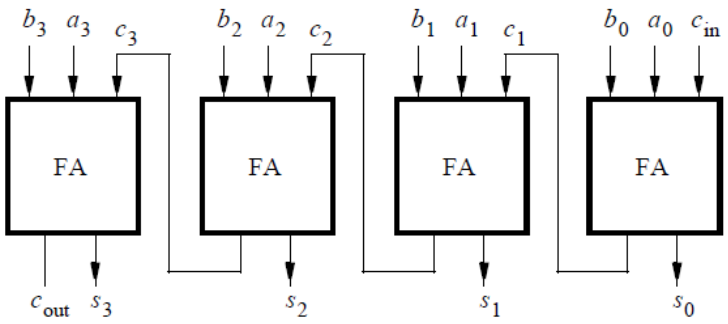
(c) Circuit

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY adder IS
        PORT (  Cin, X, Y: IN       STD_LOGIC ;
                S ,Cout  : OUT    STD_LOGIC) ;
END adder ;

ARCHITECTURE Behavior OF adder IS
BEGIN
        S <=  _____________________________________
        Cout <= _____________________________________
END Behavior ;
```



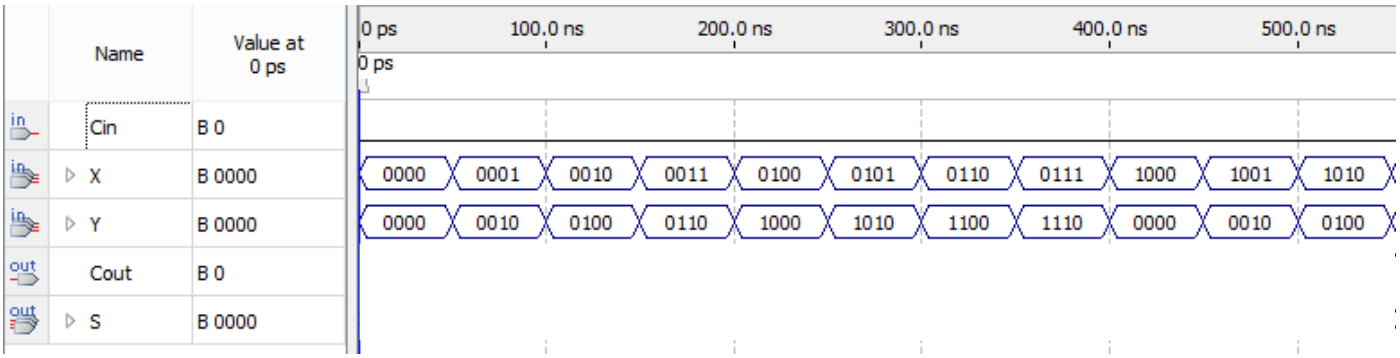
LAB 5.2 4bits ADDER using Full adder

1. Create new Project name “adder4”.
2. Create new entity for adder4 in this below



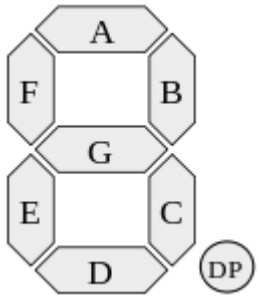
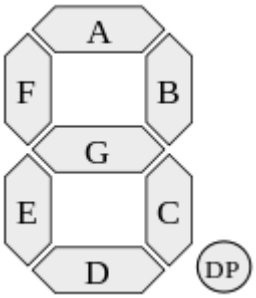
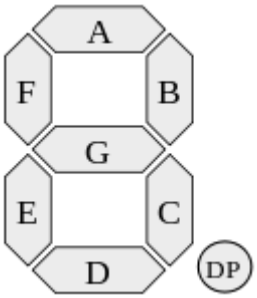
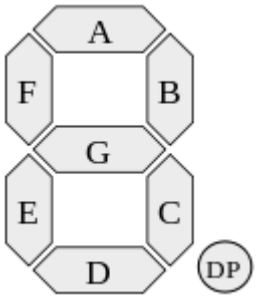
4-bits ADDER

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY adder4 IS
        PORT (  Cin     : IN    STD_LOGIC ;
                X, Y    : IN    STD_LOGIC_VECTOR(3 DOWNTO 0) ;
                S       : OUT   STD_LOGIC_VECTOR(3 DOWNTO 0) ;
                Cout    : OUT   STD_LOGIC ) ;
END adder4 ;

ARCHITECTURE Behavior OF adder4 IS
        COMPONENT adder
                PORT(   X, Y, CIn : in STD_LOGIC;
                        S, Cout : out STD_LOGIC);
         END COMPONENT;
        SIGNAL carry_sig : STD_LOGIC_VECTOR(3 DOWNTO 0) ;
BEGIN
        A1: adder port map (X(0), Y(0), Cin, S(0), carry_sig(0));
        A2: adder port map _____________________________________________
        A3: adder port map _____________________________________________
        A4: adder port map _____________________________________________
END Behavior;

--////////////////////////////////Full Adder//////////////////////////

LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY adder IS
        PORT (  Cin, X, Y: IN   STD_LOGIC ;
                S ,Cout  : OUT  STD_LOGIC) ;
END adder ;

ARCHITECTURE Behavior OF adder IS
BEGIN
        S <=  ____________________________________
        Cout <= ___________________________________
END Behavior ;
```



LAB 5.3 4bits ADDER using Full adder display with 7segment

1. Create new Project name “Lab5_3”.
2. Create new entity for adder4 to display in 7 segment

	Hex3	Hex2	Hex1	Hex0
Output	X	Y dp <= (Cout)	Display Number	
7Segment				
Input	X (SW7-4)	Y (SW3-0)		

Cin (SW8)	X (SW7-4)	Y (SW3-0)	Hex1	Hex0
0	0	5	0	5
0	4	7	1	1
0	8	5	1	3
1	7	7	1	5
1	0	0	0	1

The Truth table of 4bit display 7 segment

3. SW7-4 as Input X , SW3-0 as Input Y , SW8 as Cin
4. Use the DE0 User Manual to define the DE0 pin.
5. Compile the code and program to DE0.

This pseudo-code can change the binary number to BCD that human known.

EX. 9 = 09, A = 10, B = 11, C = 12, D = 13, E = 14, F = 15

```
S = A + B +c0
If (S > 9) then
        Z0 = 10;
        P1 = 1;
Else
        Z0 = 0;
        P1 = 0;
End if
B0 = S – Z0
B1 = P1
```

LAB 5.3 Code

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY Lab5_3 IS
        PORT (  SW : IN STD_LOGIC_VECTOR(9 DOWNTO 0);
                LEDG : OUT STD_LOGIC_VECTOR(9 DOWNTO 0);
                HEX0    : OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
                HEX1    : OUT STD_LOGIC_VECTOR(6 DOWNTO 0);
                HEX2    : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
                HEX3    : OUT STD_LOGIC_VECTOR(6 DOWNTO 0));

END Lab5_3 ;

ARCHITECTURE Behavior OF Lab5_3 IS
        COMPONENT adder
                PORT(   X, Y, CIn : in STD_LOGIC;
                        S, Cout : out STD_LOGIC);
         END COMPONENT;
         COMPONENT seg7display
                        PORT(_____________________________________________
                                ____________________________________________);
         END COMPONENT;

        SIGNAL Carry_Sig        : STD_LOGIC_VECTOR(3 DOWNTO 0) ;
        SIGNAL Cin , Cout       : STD_LOGIC ;
        SIGNAL X, Y             : STD_LOGIC_VECTOR(3 DOWNTO 0) ;
        SIGNAL S,B0,B1,Z0,P1    : STD_LOGIC_VECTOR(3 DOWNTO 0) ;

BEGIN
        LEDG <= SW;
        X <= _________________
        Y <= _________________
        Cin <= _______________
        HEX2(7) <= ____________

        A1: adder port map (X(0), Y(0), Cin, S(0), Carry_Sig(0));
        A2: adder port map ____________________________________________
        A3: adder port map ____________________________________________
        A4: adder port map ____________________________________________

        PROCESS(S)
        BEGIN
                IF (S > "1001") THEN
                        Z0 <= _______________
                        P1 <= _______________
                ELSE
                        Z0 <= _______________
                        P1 <= _______________
                END IF;
```

```
        END PROCESS;

        B0 <= _________________
        B1 <= _________________

        H1: seg7display port map (X,HEX2(6 DOWNTO 0));
        H2: seg7display port map _____________________________________________
        H3: seg7display port map _____________________________________________
        H4: seg7display port map _____________________________________________



END Behavior;

--////////////////////////////////////////////////////////////////////////////////
-- FULL ADDER

LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;

ENTITY adder IS
        PORT (  Cin, X, Y: IN       STD_LOGIC ;
                S ,Cout  : OUT    STD_LOGIC) ;
END adder ;

ARCHITECTURE Behavior OF adder IS
BEGIN
        S <=  ____________________________________________
        Cout <= ____________________________________________________
END Behavior ;

--////////////////////////////////////////////////////////////////////////////////
-- 7 Segment Display

LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY seg7display IS
        PORT(S : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
                 H : OUT STD_LOGIC_VECTOR(6 DOWNTO 0));
END seg7display;

ARCHITECTURE behavior OF seg7display IS
BEGIN
        PROCESS (S)
        BEGIN
        IF (S = "0000") THEN      H <= "1000000";  --0
        ELSIF (S = "0001") THEN  H <= "1111001";  --1
        ELSIF (S = "____") THEN  H <= "_________";  --2
        ELSIF (S = "____") THEN  H <= "_________";  --3
        ELSIF (S = "____") THEN  H <= "_________";  --4
```

```
        ELSIF (S = "____") THEN  H <= "_________";  --5
        ELSIF (S = "____") THEN  H <= "_________";  --6
        ELSIF (S = "____") THEN  H <= "_________";  --7
        ELSIF (S = "____") THEN  H <= "_________";  --8
        ELSIF (S = "____") THEN  H <= "_________";  --9
        ELSE  H <= "1111111";
        END IF;
        END PROCESS;
END behavior;
```

LAB5.3 Answer Sheet

Cin	Input X	Input Y	Cout	Hex 1	Hex0
0	0	1			
0	2	3			
0	4	5			
0	6	7			
0	8	9			
1	1	6			
1	2	7			
1	3	8			
1	4	9			
1	5	0			

Is this adder with 7segment has a limit? (If any limit, what is the limit of this lab? why? How we fix them?)

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Conclusion

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