EL323//El324 Digital System Laboratory II

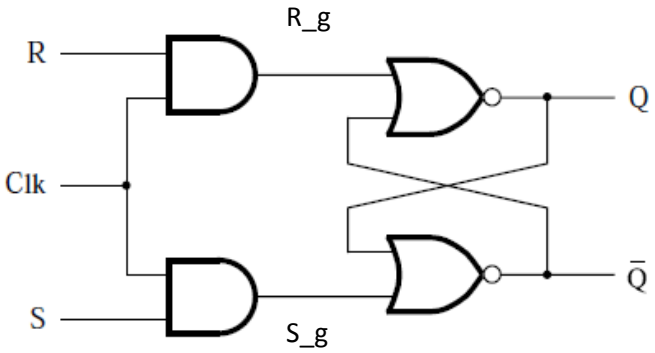
LAB 6 : D-Latch & D-Flip Flop

Objective:

1. Can use the Quartus II and create the new project using VHDL
2. To know the assign pin of DE-0 in Quartus.
3. Design using VHDL
4. To know the latch and flip flop

LAB 6.1 RS Latch

1. Create new Project name “RS_latch”.
2. Create new entity for latch in this below.



(a) Circuit

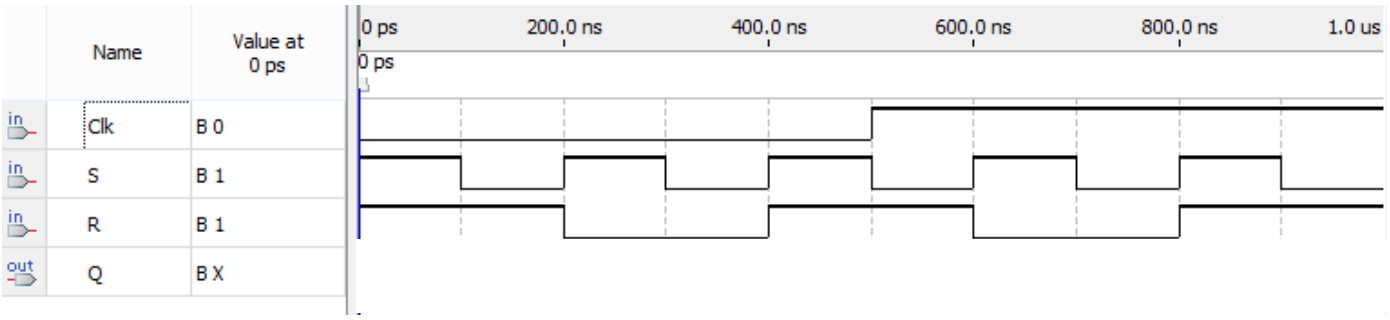
Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

(b) Characteristic table

3. Button$_0$ is clock, SW$_0$ is R and SW$_1$ is S. The Q is LED$_0$ and NQ is LED$_1$
4. Use the DE0 User Manual to define the DE0 pin.
5. Compile the code and program to DE0.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY RS_latch IS
        PORT (  Clk, R, S : IN      STD_LOGIC;
                Q,NQ    : OUT   STD_LOGIC);
END RS_latch;

ARCHITECTURE Structural OF RS_latch IS
        SIGNAL R_g, S_g, Qa, Qb : STD_LOGIC ;
        ATTRIBUTE keep: boolean;
        ATTRIBUTE keep of R_g, S_g, Qa, Qb : signal is true;
```

```
BEGIN
        R_g <=_____________________
        S_g <=_____________________
        Qa <=_____________________
        Qb <=_____________________

        Q <= Qa;
        NQ <= Qb;

END Structural;
```



Conclusion

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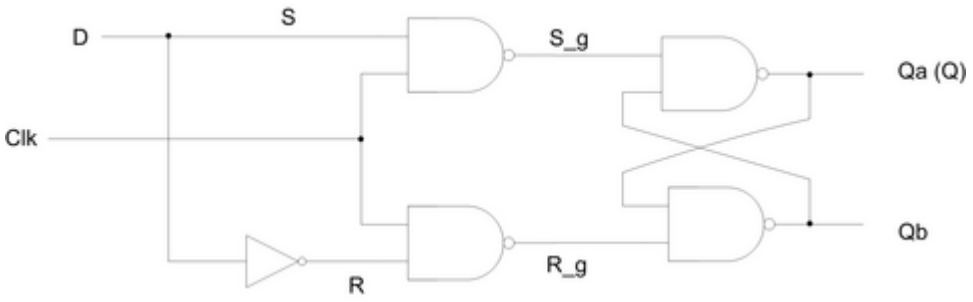
LAB6.2 D Latch

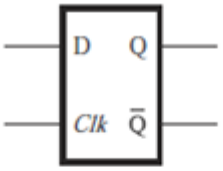
1. Create new Project name “D_latch”.
2. Create new entity for latch in this below.



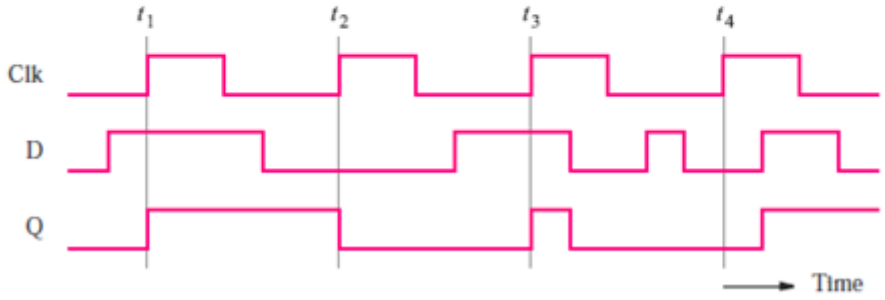
(a) Circuit

Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

(b) Characteristic table



(c) Graphical symbol



(d) Timing diagram

3. Button$_0$ is clock, SW$_0$ is D. The Q is LED$_0$ and LED Q' is LED$_1$
4. Use the DE0 User Manual to define the DE0 pin.
5. Compile the code and program to DE0.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY D_latch IS
        PORT (  Clk, D    : IN      STD_LOGIC;
                Q,NQ      : OUT     STD_LOGIC);
END D_latch;

ARCHITECTURE Structural OF D_latch IS
        SIGNAL S,R,R_g, S_g, Qa, Qb : STD_LOGIC ;
BEGIN
        S <= _____________________
        R <=_____________________
        R_g <=_____________________
        S_g <=_____________________
        Qa <=_____________________
        Qb <=_____________________
        Q <= Qa;
        NQ<=Qb;
END Structural;
```

Conclusion

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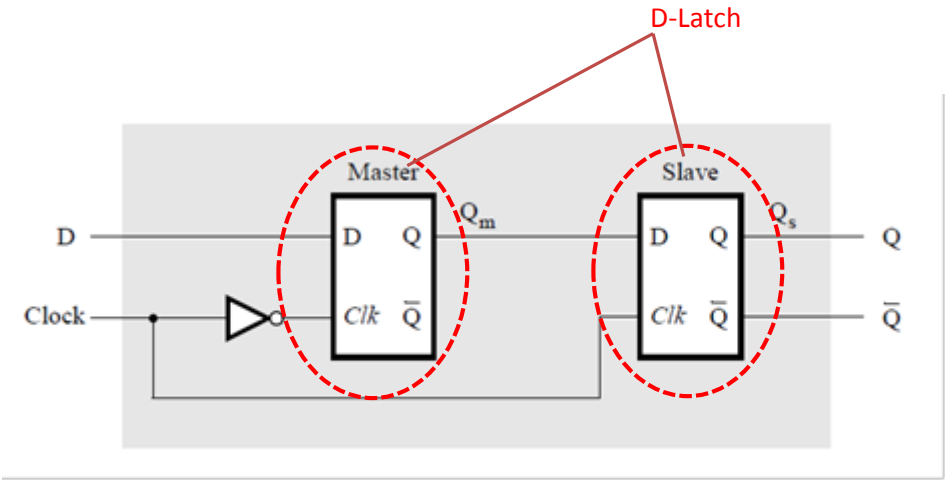
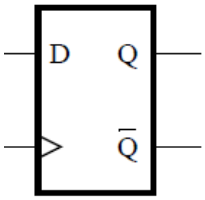
LAB6.3 Master-Slave D Flip-Flop using If-else statement.

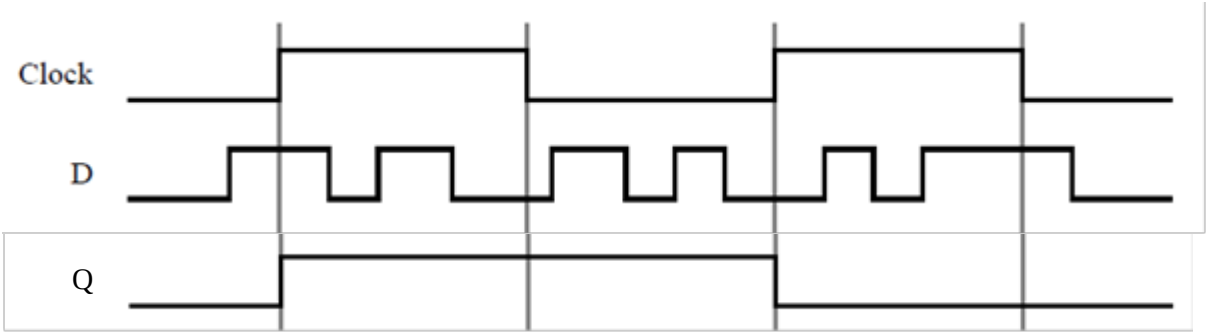
1. Create new Project name “MS_D_flipflop”.
2. Create new entity for flipflop in this below.



(a) Circuit



(b) Graphical symbol



(c) Timing diagram

3. Button$_0$ is clock, SW$_0$ is D. The Q is LED$_0$ and LED Q’ is LED$_1$ and Q$_M$ is LED$_2$
4. Use the DE0 User Manual to define the DE0 pin.
5. Compile the code and program to DE0.

Ps. The D latch would using the if-else statement

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY MS_D_flipflop IS
        PORT(   Clk, D    : IN STD_LOGIC;
                Q, Qmm  : OUT STD_LOGIC);
END MS_D_flipflop;

ARCHITECTURE Structural of MS_D_flipflop IS
        COMPONENT D_Latch
                PORT(   Clk, D    : IN      STD_LOGIC;
                        Q                 : OUT    STD_LOGIC       );
        END COMPONENT;

        SIGNAL Qm, Qs : STD_LOGIC;
BEGIN

        Master:_____________________________      -- call D-latch for MASTER
        Slave: _____________________________      -- call D-latch for SLAVE

        _____________________________________     -- set Q = Qs
        _____________________________________     -- set Qmm = Qm

END Structural;

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY D_latch IS
        PORT (  Clk, D    : IN      STD_LOGIC;
                Q                 : OUT    STD_LOGIC       );
END D_latch;

ARCHITECTURE Structural OF D_latch IS
        SIGNAL Qa: STD_LOGIC;
BEGIN
        PROCESS (D, Clk)
        BEGIN
                _________________     -- The D latch  in if-else statement
                _________________
                _________________
        END PROCESS;

        Q <= Qa;

END Structural;
```

Conclusion

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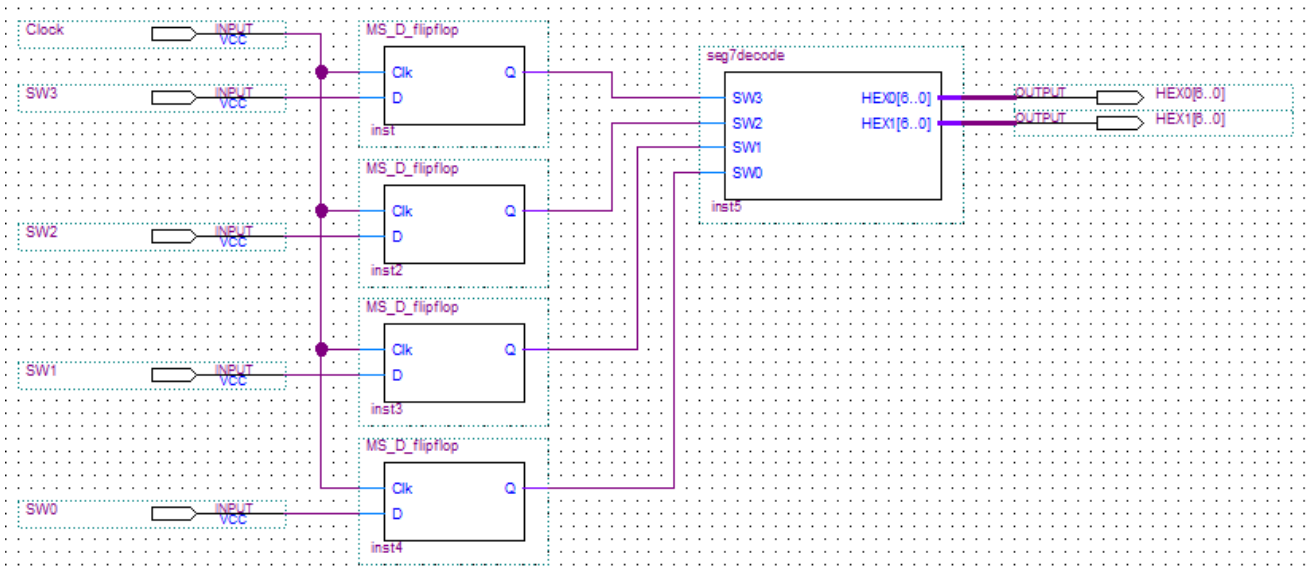
LAB6.4 Using the Master-Slave D Flipflop to store the data.

1. Create new Project name “7seg_d_flipflop”.
2. Create new entity for flipflop in this below.
3. $Button_0$ is clock, SW_{3-0} are input A, SW_{7-4} are input B. The Hex_{3-2} are Output of A and the Hex_{1-0} are Output of B.
4. Use the DE0 User Manual to define the DE0 pin.
5. Compile the code and program to DE0.



Conclusion

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The seg7decode is shown in below. It like the real number call BCD that human know. (Lab5.3)