EL323//El324 Digital System Laboratory II

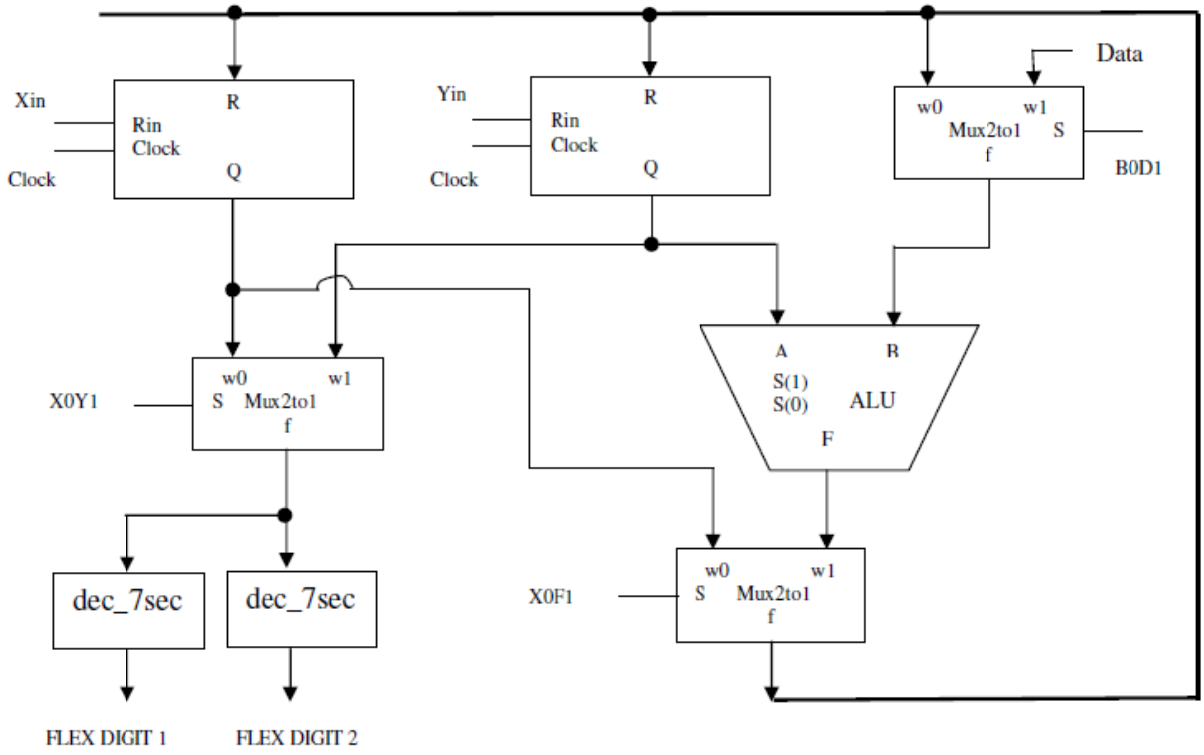
LAB 9:Register Transfer Logic (RTL) and Bus

Objective:

1. Can use the Quartus II and create the new project using VHDL
2. To know the assign pin of DE-0 in Quartus.
3. Design using VHDL
4. To know the RTL and Bus.

LAB 9.1ALU8BITS VHDL CODE

1. Create new Project name “RTL”.
2. Create new entity for RTL in this below.



Connect	To
Data[3..0]	Sw[3 downto 0]
Opcode[1..0]	Sw[9 downto 8]
Xin	Sw7
Yin	Sw6
X0F1	Sw5
X0Y1 (Display x,y)	Sw4
B0D1	Button1
Clock	Button2
Dec_7	Hex0 and Hex1

The define of Switch and button to show the 7segdisplay.

Opcode(1)	Opcode(0)	ALU_OUTPUT	Operation
0	0	0	Clear
0	1	A + B	Add
1	0	A – B	Substact
1	1	B	Load B

3. Use the DE0 User Manual to define the DE0 pin.
4. Compile the code and program to DE0.

Result

SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	BT2	BT1	Hex1	Hex0
0	0	0	0	0	0	0	0	0	0	clk	1		
1	1	0	1	1	1	0	0	1	0	clk	1		
1	1	1	0	1	0	0	1	1	0	clk	1		
x	x	x	x	x	1	x	x	x	x	x	x		
1	0	1	0	1	0	1	0	0	0	clk	1		
x	x	x	x	x	1	x	x	x	x	x	x		
1	0	1	0	1	0	0	1	1	1	clk	1		
x	x	x	x	x	1	x	x	x	x	x	x		
0	0	0	1	0	0	0	1	1	1	clk	1		
x	x	x	x	x	1	x	x	x	x	x	x		
0	1	0	1	1	1	0	0	1	1	clk	1		
0	0	0	1	0	1	0	0	0	0	clk	1		
x	x	x	x	x	0	x	x	x	x	x	x		

Conclusion

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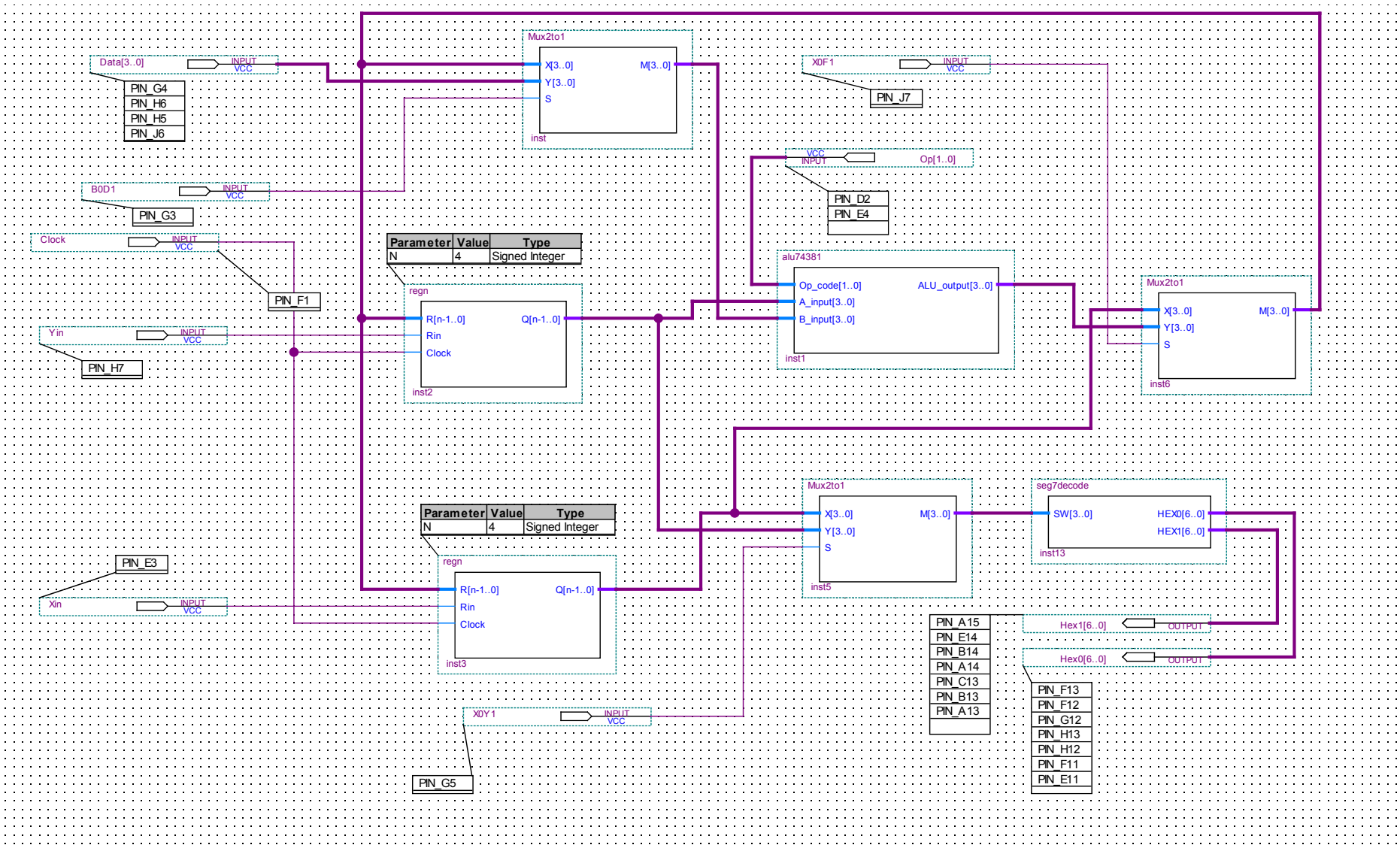
Code For “regn”

```
library ieee;
use ieee.std_logic_1164.all;


entity regn is
        generic( N : integer := 4 );
        port(
                R : IN std_logic_vector(N-1 DOWNTO 0);
                Rin, Clock : IN std_logic;
                Q : OUT std_logic_vector(N-1 DOWNTO 0)
        );
end regn;

architecture behavior of regn is
begin
        process
                 begin
                wait until Clock'EVENT and Clock = '1';
                 if Rin = '1' then
                        Q <= R;
                end if;
        end process;
end behavior;
```


Mux2to1
X[3..0]
Y[3..0]
S
M[3..0]
inst
Data[3..0]
INPUT
VCC
PIN_G4
PIN_H6
PIN_H5
PIN_J6
X0F1
PIN_J7
B0D1
PIN_G3
Op[1..0]
PIN_D2
PIN_E4
Clock
PIN_F1
Parameter Value Type
N 4 Signed Integer
regn
R[n-1..0]
Rin
Clock
Q[n-1..0]
inst2
alu74381
Op_code[1..0]
A_input[3..0]
B_input[3..0]
ALU_output[3..0]
inst1
Yin
PIN_H7
inst6
PIN_E3
Xin
inst3
inst5
seg7decode
SW[3..0]
HEX0[6..0]
HEX1[6..0]
inst13
PIN_A15
PIN_E14
PIN_B14
PIN_A14
PIN_C13
PIN_B13
PIN_A13
Hex1[6..0]
Hex0[6..0]
OUTPUT
PIN_F13
PIN_F12
PIN_G12
PIN_H13
PIN_H12
PIN_F11
PIN_E11
X0Y1
PIN_G5